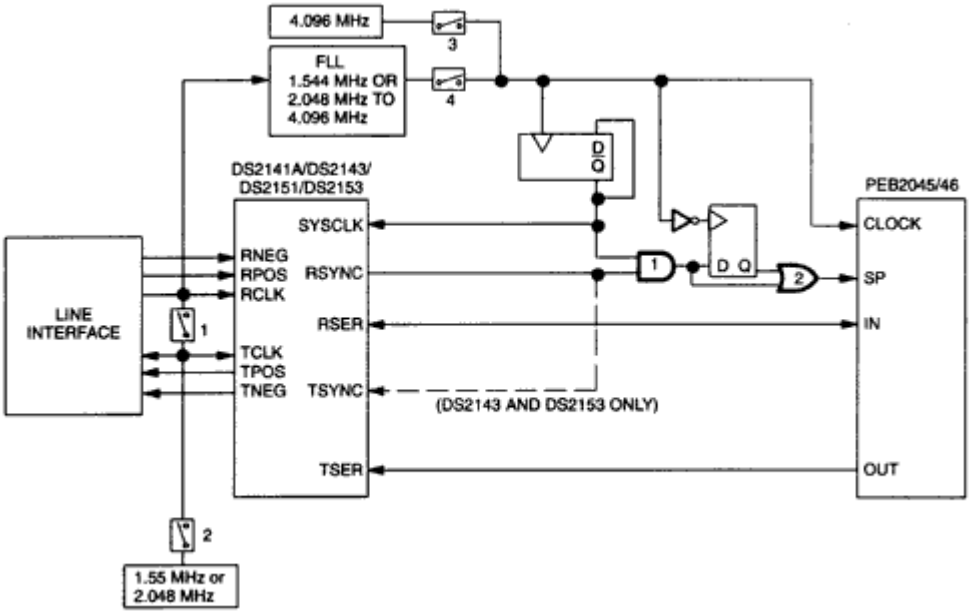
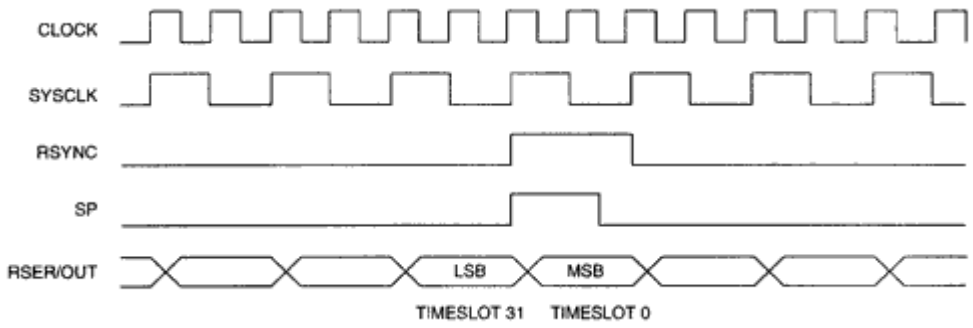
App Note 315: DS2141A, DS2143, DS2151, DS2153 Interfacing to the Siemens PEB2045

This application note describes how the DS2141A, DS2143, DS2151, and DS2153 interface to the Siemens PEB2045. This note also shows waveforms and timing diagrams of different pins that are used for interfacing to the PEB2045.



Notes:

1. The PEB2045 is operated in the 4 MHz standard configuration mode.
2. Gates #1 and #2 are used to condition the frame sync to meet the timing requirements of the PEB2045.
3. Both the transmit and receive elastic stores in the DS2141A, DS2151 are enabled; the DS2143, DS2153 only need the receive side elastic store enabled.
4. The DS2141A, DS2151 is set up to output a frame sync at the RSYNC and TSYNC pins while the DS2143, DS2153 is set up to output a frame sync at RSYNC and input a frame sync at TSYNC.
5. The DS2141A, DS2143, DS2151 and DS2153 is set up for SYSCLK operation of 2.048 MHz.
6. The elastic stores provide controlled slip operation.
7. In "looped-timed" applications, close switch 1 and open switch 2.
8. In applications that cannot handle controlled slips, close switches 1 and 4 and open switches 2 and 3.
9. In DS2151 and DS2153 applications, the line interface block is included onboard the device.
10. Timing between the devices is shown below:



MORE INFORMATION

DS2141A:	QuickView	-- Full (PDF) Data Sheet (480k)	-- Free Sample
DS2143:	QuickView	-- Full (PDF) Data Sheet (568k)	-- Free Sample